REMARKS

In Section 1 of the Office Action, the Examiner objected to the title of the invention as being non-descriptive. Applicant has amended the title to be more clearly indicative of the invention to which the claims are directed.

In Section 2 of the Office Action, claim 1 was objected to for containing a minor error. With this Amendment, Applicant has corrected the error. Withdrawal of the objection is respectfully requested.

In Section 4 of the Office Action, the Examiner rejected claims 1, 2, 4 and 5 under 35 U.S.C. §102(e) as being anticipated by Borel (U.S. Patent No. 6,130,460). Applicant respectfully disagrees with the rejections for the reasons set forth below.

The present invention is directed to a hard macro for use in an Application Specific Integrated Circuit (ASIC) that prevents antenna rule violations from occurring altogether when used to form an integrated circuit. As a result, the present invention not only eliminates the need to perform checks for violations of antenna rules, but also eliminates the need to perform fixes to the hard macro design. As explained in the background of the application, hard macros are components that can be dropped into the circuit layout to perform a desired function, such as processors, including processor cores, memory arrays, input and output interface circuits, encoders, decoders, and other types of circuit blocks. In other words, hard macros are drop-in predefined components that are used to form integrated circuits.

Borel neither teaches nor suggests the hard macro design of the present invention. Instead, Borel is directed to a process for producing an integrated circuit, is initially defined without regard to antenna rule violations. [Column 3, Lines 8-12] Accordingly, checks must be made to determine whether any such

violations exist. [Id.] Borel then teaches a method of fixing the violations, once discovered, substantially in the manner discussed in the background of the present application. Accordingly, Borel provides no teaching or suggestion of the hard macro design of the present invention that can be used in the formation of an integrated circuit and includes improved port routing that eliminates the possibility of antenna rule violations thereby eliminating the need to perform the checks and fixes taught by Borel.

The Examiner submits that the EMP point of Borel is equivalent to the "input/output (I/O) port" of claim 1 of the present application and cites column 6, lines 3-12 as further support for the contention which reads as follows:

> With regard to the definition of the general design diagram of the integrated circuit, and, more particularly, of the initial geometrical configuration of the track PCN, a point EMP located is selected at a sight compatible with the general design diagram of the integrated circuit (more particularly, the layer M2). The point EMP furthermore lies at a distance L2 from gate GR less than the critical length, and preferably is as close as possible to the gate of the transistor. The point EMP is selected from within the first track element EL1, for example, directly by the CAD tool which has a name of the general integrated-circuit diagram to be established.

Accordingly, there is no teaching or suggestion in Borel that the cited point EMP is a I/O port of a hard macro as described in independent claim 1.

The Examiner also submits that Borel teaches the "top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region" in claim 1 at

column 5, lines 63-67 of Borel. The cited language of Borel reads:

> Likewise, the conventional production of the diffusion barrier layers, for example made of TiN arranged between aluminum metallization levels and tungsten vias will not be described below, for the sake of simplification.

Applicant respectfully submits that the cited disclosure fails to teach or even suggest the top level metallic conductor of a hard macro as defined in claim 1.

Finally, the Examiner submits that the "electrical connection" of claim 1 is taught by Borel at column 5, lines 30-34, which reads:

> The second end of the track element EL1 and the first end of the track element EL2 are respectively connected by two vias to a track element ELS of the metallization level M2 above, which in this case is the highest metallization level.

Applicant respectfully submits that the cited disclosure relates to FIG. 1 of Borel and illustrates a design that violates an antenna rule. (See column 5, lines 35-44) Borel then discusses a method of fixing antenna rule violations in accordance with the invention. Furthermore, neither of the track elements correspond to the "input/output port" of the present invention.

Accordingly, Applicant respectfully believes that independent claim 1 is allowable since the cited reference fails to teach the invention as claimed. Applicant, therefore, requests that the rejection of claim 1 be withdrawn. Applicant further requests that the rejections of claims 2 and 4 be withdrawn since they depend from allowable base claim 1.

In section 8 of the Office Action, the Examiner rejected claim 5, which is generally directed to a method of producing the hard macro of claim 1. As discussed above, Borel fails to teach the hard macro of the present invention. In particular, the method of Borel relates to fixing antenna rule violations of an existing integrated circuit, which is unrelated to the method of forming the hard macro of the present invention that avoids the antenna rule violations altogether. Thus, in accordance with the discussion with respect to independent claim 1, Applicant respectfully believes that independent claim 5 is allowable and requests that the rejection be withdrawn.

In Section 11 of the Office Action, the Examiner rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Borel and Applicant's admitted prior art. Applicant respectfully believes that claim 3 is allowable since it depends from claim 1, which is believed to be allowable for the reasons set forth above. Applicant, therefore, requests that the rejection be withdrawn.

In view of the above comments and remarks, it is believed that the present application is in condition for allowance. Consideration and favorable action is respectfully requested.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

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BDK/djb

MARKED-UP VERSION OF REPLACEMENT PARAGRAPHS

Replacement title for the title on Page 1, line 1 and the title located in the Abstract on Page 13, line 1:

HARD MACRO HAVING IMPROVED PORT ROUTING FOR AVOIDANCE OF ANTENNA RULE VIOLATIONS

MARKED-UP VERSION OF REPLACEMENT CLAIMS

1. A hard macro for use in an Application Specific Integrated Circuit (ASIC), comprising:

an input/output (I/O) port having a port level metallic conductor ~~of~~in a low level metalization layer;

an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

a top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region; and

an electrical connection between the port level metallic conductor and the gate conductor including a first conducting section extending from the gate conductor to the top level metallic conductor and a second conducting section extending from the top level metallic conductor to the port level conductor.